CLAIMS

We claim:

1. A circuit, comprising:

a source of a limited current connected to a first node;

a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node to provide a level-shifted output signal at the first node; and

a second semiconductor device, having an input connected to an input signal, and having an output connected to the second node.

2. The circuit of claim 1 wherein the source of a limited current is a semiconductor device which performs as a weak current source.

3. The circuit of claim 1 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein the second semiconductor device is not rated to withstand the predetermined voltage.

4. The circuit of claim 1 wherein the first semiconductor device is a metal oxide semiconductor transistor connected in a source-follower configuration.

5. The circuit of claim 1 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected to the bias voltage, the drain being connected to the first node, and the source being connected to the second node.

6. A circuit, comprising:

a source of a limited current connected to a first node;

a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node to provide an output signal at the first node;

a second semiconductor device, having an input connected to an input signal, and having an output connected to the second node; and

a driver having an input connected to the first node and having an output to provide a level-shifted output signal.

7. The circuit of claim 6 wherein the source of a limited current is a semiconductor device which performs as a weak current source.

8. The circuit of claim 6 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein the second semiconductor device is not rated to withstand the predetermined voltage.

9. The circuit of claim 6 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device and the driver are rated to withstand the predetermined voltage, and wherein the second semiconductor device is not rated to withstand the predetermined voltage.

10. The circuit of claim 6 wherein the first semiconductor device is a metal oxide semiconductor transistor connected in a source-follower configuration.

11. The circuit of claim 6 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected

to the bias voltage, the drain being connected to the first node, and the source being connected to the second node.

12. A circuit, comprising:

a source of a limited current connected to a first node;

a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node to provide a level-shifted output signal at the first node; and

a plurality of second semiconductor devices, the plurality being in a series-connected configuration, one end of the plurality being connected to the second node, each second semiconductor device of the plurality of second semiconductor devices having an input connected to a corresponding one of a plurality of input signals.

13. The circuit of claim 12 wherein the source of a limited current is a semiconductor device which performs as a weak current source.

14. The circuit of claim 12 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein at least one second semiconductor device of the plurality of second semiconductor devices is not rated to withstand the predetermined voltage.

15. The circuit of claim 12 wherein the first semiconductor device is a metal oxide semiconductor transistor connected in a source-follower configuration.

16. The circuit of claim 12 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected to the predetermined voltage, the drain being connected to the first node, and the source being connected to the second node.

17. A circuit, comprising:

a source of a limited current connected to a first node;

a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node;

a plurality of second semiconductor devices, the plurality being in a series-connected configuration, one end of the plurality being connected to the second node, each second semiconductor device of the plurality of second semiconductor devices having an input connected to a corresponding one of a plurality of input signals; and

a driver, having an input connected to the first node, and having an output to provide a level-shifted output signal.

18. The circuit of claim 17 wherein the source of a limited current is a semiconductor device which performs as a weak current source.

19. The circuit of claim 17 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein at least one second semiconductor device of the plurality of second semiconductor devices is not rated to withstand the predetermined voltage.

20. The circuit of claim 17 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device and the driver are rated to withstand the predetermined voltage, and wherein at least one second semiconductor device of the plurality of second semiconductor devices is not rated to withstand the predetermined voltage.

21. The circuit of claim 17 wherein the first semiconductor device is a metal oxide semiconductor transistor connected in a source-follower configuration.

22. The circuit of claim 17 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected to the predetermined voltage, the drain being connected to the first node, and the source being connected to the second node.

23. A memory, comprising:

a control circuit to provide a first signal, the first signal having a first voltage;

a source of a limited current connected to a first node;

a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node to provide a second signal at the first node, the second signal having a second voltage, the second voltage being greater than the first voltage;

a second semiconductor device, having an input connected to the control circuit and responsive to the first signal from the control circuit, and having an output connected to the second node; and

a memory cell responsive to the second signal.

24. The circuit of claim 23 wherein the source of a limited current is a semiconductor device which performs as a weak current source.

25. The circuit of claim 23 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein the second semiconductor device is not rated to withstand the predetermined voltage.

26. The circuit of claim 23 wherein the first semiconductor device is a metal oxide semiconductor transistor connected in a source-follower configuration.

27. The circuit of claim 23 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected to the predetermined voltage, the drain being connected to the first node, and the source being connected to the second node.

28. A memory, comprising:

a control circuit to provide a first signal, the first signal having a first voltage;

a source of a limited current connected to a first node;

a first semiconductor device having an input connected to a bias voltage, being connected between the first node and a second node;

a second semiconductor device, having an input connected to the control circuit and responsive to the first signal from the control circuit, and having an output connected to the second node; and

a driver having an input connected to first node and an output to provide a second signal, the second signal having a second voltage, the second voltage being greater than the first voltage; and

a memory cell responsive to a second signal.

29. The circuit of claim 28 wherein the source of a limited current is a semiconductor device which performs as a weak current source.

30. The circuit of claim 28 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein the second semiconductor device is not rated to withstand the predetermined voltage.

31. The circuit of claim 28 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device and the driver are rated to withstand the predetermined voltage, and wherein the second semiconductor device is not rated to withstand the predetermined voltage.

32. The circuit of claim 28 wherein the first semiconductor device is a metal oxide semiconductor transistor connected in a source-follower configuration.

33. The circuit of claim 28 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected to the predetermined voltage, the drain being connected to the first node, and the source being connected to the second node.

34. A memory, comprising:

a control circuit to provide a plurality of first signals, at least one signal of the plurality of first signals having a first voltage;

a source of a limited current connected to a first node;

a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node to provide a second signal at the second node, the second signal having a second voltage, the second voltage being greater than the first voltage;

a plurality of second semiconductor devices, the plurality being in a series-connected configuration, one end of the plurality being connected to the second node, each second semiconductor device of the plurality of second semiconductor devices having an input connected to a corresponding first signal of the plurality of first signals; and

a memory cell responsive to a second signal.

35. The circuit of claim 34 wherein the source of a limited current is a semiconductor device which performs as a weak current source.

36. The circuit of claim 34 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein at least one second semiconductor device of the plurality of second semiconductor device is not rated to withstand the predetermined voltage.

37. The circuit of claim 34 wherein the first semiconductor device is a metal oxide semiconductor transistor connected in a source-follower configuration.

38. The circuit of claim 34 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected to the predetermined voltage, the drain being connected to the first node, and the source being connected to the second node.

39. A memory, comprising:

a control circuit to provide a plurality of first signals, at least one signal of the plurality of first signals having a first voltage;

a source of a limited current connected to a first node;

a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node;

a plurality of second semiconductor devices, the plurality being in a series-connected configuration, one end of the plurality being connected to the second node, each second semiconductor device of the plurality of second semiconductor devices having an input connected to a corresponding first signal of the plurality of first signals;

a driver having an input connected to first node and an output to provide the second signal, the second signal having a second voltage, the second voltage being greater than the first voltage; and

a memory cell responsive to the second signal.

40. The circuit of claim 39 wherein the source of a limited current is a semiconductor device which performs as a weak current source.

41. The circuit of claim 39 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device is rated to withstand the predetermined voltage, and wherein at least one second semiconductor device of the plurality of second semiconductor devices is not rated to withstand the predetermined voltage.

42. The circuit of claim 39 wherein the source of a limited current is connected to a predetermined voltage, wherein the first semiconductor device and the driver are rated to withstand the predetermined voltage, and wherein at least one second semiconductor device of the plurality of second semiconductor devices is not rated to withstand the predetermined voltage.

43. The circuit of claim 39 wherein the first semiconductor device is a metal oxide semiconductor transistor connected in a source-follower configuration.

44. The circuit of claim 39 wherein the first semiconductor device is a metal oxide semiconductor transistor having a gate, a drain, and a source, the gate being the input connected to the predetermined voltage, the drain being connected to the first node, and the source being connected to the second node.